

CLAIMS

1. (original) A receiver for a received signal having two or more data levels, the received signal having been transmitted over a transmission channel, the receiver comprising:
- (a) two or more channel estimators, at least one channel estimator for each different data level for the received signal, each channel estimator being configured to model the transmission channel to generate an estimated signal corresponding to one of the data levels; and
 - (b) a comparator configured to (1) receive the received signal and the estimated signal from each channel estimator and (2) select an output data level for the received signal.
2. (original) The receiver of claim 1, wherein each channel estimator implements a 2nd order or higher model of the transmission channel.
3. (original) The receiver of claim 2, wherein the model is an adaptive model of the transmission channel that is dynamically controlled based on an error signal generated by the comparator.
4. (original) The receiver of claim 2, wherein each channel estimator comprises a processing path for each order term in the model of the transmission channel.
5. (original) The receiver of claim 4, wherein at least one of the processing paths in each channel estimator comprises a multiplication node having an adaptive coefficient that is dynamically controlled based on an error signal generated by the comparator.
6. (original) The receiver of claim 5, wherein a processing path in each channel estimator corresponding to a 1st order term of the model with a coefficient having a value of 1, wherein the 1st order term processing path is implemented without a multiplication node.
7. (currently amended) The receiver of claim 1, ~~wherein the two or more channel estimators comprise~~ further comprising one or more adaptive equalizers, each adaptive equalizer configured to receive ~~a current an ideal~~ data level signal corresponding to one of the data levels and to generate an input signal for one or more of the channel estimators.
8. (original) The receiver of claim 7, wherein at least one adaptive equalizer is shared by two or more of the channel estimators.
9. (original) The receiver of claim 8, wherein all of the channel estimators share a single adaptive equalizer.
10. (original) The receiver of claim 7, wherein each adaptive equalizer is further configured to receive one or more future data levels and the receiver comprises a channel estimator for each different combination of current and future data levels.
11. (original) The receiver of claim 7, wherein tap data for each adaptive equalizer corresponds to sliced symbols corresponding to the two or more data levels.
12. (original) The receiver of claim 1, wherein the comparator comprises:
- (a) a subtraction node for each channel estimator configured to generate a difference signal between the received signal and the corresponding estimated signal; and

4 (b) a compare-and-select module configured to receive the difference signals from the
5 subtraction nodes and to select the output data level for the received signal based on a difference signal
6 having a smallest absolute value.

1 13. (original) The receiver of claim 1, wherein:
2 the transmission channel is an optical transmission channel; and
3 the two or more channel estimators and the comparator are implemented in a single integrated
4 circuit as analog circuitry.

1 14. (original) A method for processing a received signal having two or more data levels, the
2 received signal having been transmitted over a transmission channel, the method comprising the steps of:

3 (a) generating at least one estimated signal for each data level based on a model of the
4 transmission channel; and

5 (b) processing the received signal and the estimated signal for each data level to select an
6 output data level for the received signal.

1 15. (original) The method of claim 14, wherein step (a) comprises the step of implementing
2 a 2nd order or higher model of the transmission channel.

1 16. (original) The method of claim 15, wherein the model is an adaptive model of the
2 transmission channel that is dynamically controlled based on an error signal generated during step (b).

1 17. (original) The method of claim 14, further comprising the steps of:

2 (c) generating a difference signal between the received signal and the corresponding
3 estimated signal; and

4 (d) selecting the output data level for the received signal based on a difference signal having
5 a smallest absolute value.

1 18. (new) The receiver of claim 2, wherein the model of the transmission channel includes
2 at least one of a 0th order term and a 1st order term.

1 19. (new) The receiver of claim 18, wherein each channel estimator comprises a processing
2 path for each order term in the model of the transmission channel.

1 20. (new) The receiver of claim 7, wherein each channel estimator receives a different input
2 signal from the one or more adaptive equalizers.

1 21. (new) A receiver for a received signal having two or more data levels, the received
2 signal having been transmitted over a transmission channel, the receiver comprising:

3 (a) an adaptive equalizer, a corresponding channel estimator, and a corresponding
4 subtraction node for each data level; and

5 (b) a compare-and-select module, wherein:

6 each adaptive equalizer is configured to receive an ideal data level signal for the
7 corresponding data level and to generate an input signal for the corresponding channel estimator;

8 each channel estimator is configured to model the transmission channel to generate an
9 estimated signal corresponding to said each data level, each channel estimator implementing a 2nd order
10 or higher model of the transmission channel, wherein:

11 the model has at least a 0th order term, a 1st order term, and a 2nd order term; and
12 said each channel estimator comprises a processing path for each order term in
13 the model;

14 each subtraction node is configured to generate a difference signal between the received
15 signal and the corresponding estimated signal; and
16 the compare-and-select module configured to receive the difference signals from the
17 subtraction nodes and to select the output data level for the received signal based on a difference signal
18 having a smallest absolute value.

1 22. (new) A receiver for a received signal having two or more data levels, the received
2 signal having been transmitted over a transmission channel, the receiver comprising:

3 (a) an adaptive equalizer;
4 (b) a set of ideal-data-level circuitry, a corresponding channel estimator, and a
5 corresponding subtraction node for each data level; and
6 (b) a compare-and-select module, wherein:
7 the adaptive equalizer is configured to generate a single adapted equalizer signal for each
8 set of ideal-data-level circuitry;

9 each set of ideal-data-level circuitry is configured to receive an ideal signal data level for
10 the corresponding data level and to generate an input signal for the corresponding channel estimator;

11 each channel estimator is configured to model the transmission channel to generate an
12 estimated signal corresponding to said each data level, each channel estimator implementing a 2nd order
13 or higher model of the transmission channel, wherein:

14 the model has at least a 0th order term, a 1st order term, and a 2nd order term; and
15 said each channel estimator comprises a processing path for each order term in
16 the model;

17 each subtraction node is configured to generate a difference signal between the received
18 signal and the corresponding estimated signal; and

19 the compare-and-select module configured to receive the difference signals from the
20 subtraction nodes and to select the output data level for the received signal based on a difference signal
21 having a smallest absolute value.

REMARKS/ARGUMENTS

Claims 1-17 were previously pending in the application. Claim 7 is amended; and new claims 18-22 are added herein. Support for new claims 18-20 is found in both Figs. 2 and 3, support for new claim 21 is found in Fig. 2, and support for new claim 22 is found in Fig. 3. Assuming the entry of this amendment, claims 1-22 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

35 U.S.C. 112, First Paragraph

In paragraph 1 of the office action, the Examiner rejected claims 1-17 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. In particular, referring to both claims 1 and 14, the Examiner stated that the specification does not disclose "a comparator receiving the received signal and the estimated signal from each channel estimator."

In response, the Applicant submits that, for example, in the embodiment shown in Fig. 2, the comparator comprises subtraction nodes 215 and 216 and compare-and-select module 217. This interpretation is explicitly supported in the specification on page 3, lines 18-19. This is also supported by claim 12, which explicitly recites that the comparator of claim 1 comprises a subtraction node for each channel estimator and a compare-and-select module.

Given this interpretation of the term "comparator" as used in claim 1, it is clear that the specification does indeed provide a written description of a comparator that receives both the received signal (e.g., v_{in} of Fig. 2) and the estimated signal from each channel estimator (e.g., signals from summation nodes 213 and 214).

The Applicant notes further that claim 14 is a method claim that recites "processing the received signal and the estimated signal for each data level to select an output data level for the received signal." Significantly, claim 14 does not even recite the term "comparator."

For all these reasons, the Applicant submits that the rejections of the claims based on Section 112, first paragraph, have been overcome.

Prior Art Rejections

In paragraph 2, the Examiner rejected claims 1-2, 4, 7-12, 14-15, and 17 under 35 U.S.C. 102(b) as being anticipated by Shiokawa. In paragraph 3, the Examiner rejected claim 13 under 35 U.S.C. 103(a) as being unpatentable over Shiokawa. In paragraph 4, the Examiner rejected claims 3 and 16 under 35 U.S.C. 103(a) as being unpatentable over Shiokawa in view of Applicant's Admitted Prior Art (AAPA). In paragraph 5, the Examiner objected to claims 5-6 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form. For the following reasons, the Applicant submits that all of the now-pending claims are allowable over the cited references.

Claim 1

Claim 1 is directed to a receiver for a received signal having two or more data levels. The receiver has two or more channel estimators and a comparator. Each channel estimator is configured to model the transmission channel to generate an estimated signal corresponding to one of the data levels.

The comparator is configured to (1) receive the received signal and the estimated signal from each channel estimator and (2) select an output data level for the received signal. The Applicant submits that Shiokawa does not teach such a combination of features.

As shown in Fig. 1, Shiokawa teaches a signal processor having an adaptive equalizer 1, a maximum likelihood estimator 2, and a (1+D) demodulator 3. Maximum likelihood estimator 2 includes subtractors 30-34, squaring circuits 35-39, add-compare-select (ACS) circuit 5, and path memory 6.

In rejecting claim 1, the Examiner stated that Shiokawa discloses two or more channel estimators, citing subtractors 30-34 in Fig. 1. The Examiner also stated that Shiokawa discloses “a comparator (5) configured to receive the *signals from the channel estimators* and select and output data level for the received signal,” citing column 4, lines 10-52. Significantly, in rejecting claim 1, the Examiner omitted part of the explicit recitations of claim 1.

According to claim 1, the comparator receives “the received signal and the estimated signal from each channel estimator.” In rejecting claim 1, the Examiner did not state that the comparator of Shiokawa receives the received signal. There is good reason for this omission. The fact is that ACS circuit 5 taught in Shiokawa does not receive the received signal. As such, Shiokawa does not teach the features explicitly recited in claim 1.

There is no way to interpret the teachings of Shiokawa to fall within the scope of claim 1. According to Shiokawa, “each subtractor and the corresponding squaring circuit form a likelihood estimator for producing a likelihood value B.” See column 4, lines 13-14. Assuming only for the sake of argument that these likelihood estimators in Shiokawa are examples of the channel estimators of claim 1, then Shiokawa fails to teach the comparator of claim 1, because ACS circuit 5 of Shiokawa does not receive the received signal; it receives only the branch metrics B from the squaring circuits. (Ironically, this argument is similar to the Examiner’s own argument for rejecting claim 1 under 35 U.S.C. 112, first paragraph.)

The other possible interpretation of the teachings of Shiokawa is that Shiokawa’s maximum likelihood estimator 2 is an example of a comparator that receives both the received signal (i.e., from adaptive equalizer 1) and signals corresponding to the different data levels (i.e., +1.5, +1, 0, -1, and -1.5). According to this interpretation, Shiokawa’s subtractor 30-34 may be said to be analogous to subtractors 215 and 216 of Fig. 2 of the present application, and Shiokawa’s ACS circuit 5 may be said to be analogous to compare-and-select circuit 217 of the present application.

Under this second interpretation, however, Shiokawa fails to teach examples of the two or more channel estimators explicitly recited in claim 1. In Shiokawa, the input to the subtractors are exact signal levels (i.e., +1.5, +1, 0, -1, and -1.5). In Shiokawa, there is no modeling of the transmission channel to generate an estimated signal corresponding to each ideal signal level signal (as explicitly recited in claim 1).

The Examiner cannot have it both ways. Either Shiokawa does not teach the comparator of claim 1 or Shiokawa does not teach the channel estimators of claim 1.

For all these reasons, the Applicant submits that claim 1 is allowable over Shiokawa. For similar reasons, the Applicant submits that claim 14 is allowable over Shiokawa. Since claims 2-13 and 15-20 depend variously from claims 1 and 14, it is further submitted that those claims are also allowable over Shiokawa.

Claims 3 and 16

According to claim 2, each channel estimator implements a 2nd order or higher model of the transmission channel. According to claim 3, which depends from claim 2, the model is an adaptive model of the transmission channel that is dynamically controlled based on an error signal generated by the comparator.

In rejecting claim 2, the Examiner cited squaring circuits 35-39 in support of his conclusion that Shiokawa teaches that each channel estimator in Shiokawa implements a 2nd order model of the transmission channel. In rejecting claim 3, the Examiner cited AAPA. In particular, the Examiner stated that AAPA discloses slicer 108 of Fig. 1 (having a similar function to Shiokawa's ACS circuit 5), where slicer 108 generates an error signal that is fed back to equalizer 102 of Fig. 1 (having a similar function to Shiokawa's adaptive equalizer 1).

Assuming for the sake of argument that the Examiner is correct that (a) AAPA's slicer 108 has a similar function to Shiokawa's ACS circuit 5 and (b) AAPA's equalizer 102 has a similar function to Shiokawa's adaptive equalizer 1, that still does not make claim 3 obvious.

According to claim 3, the channel estimator implements a 2nd order or higher adaptive model that is dynamically controlled based on an error signal generated by the comparator. The Examiner concluded that squaring circuits 35-39 are examples of a 2nd order model of the transmission channel. But those squaring circuits are not part of Shiokawa's adaptive equalizer 1. As such, a suggestion in AAPA that an adaptive equalizer analogous to Shiokawa's adaptive equalizer 1 is controlled based on an error signal fed back from a slicer analogous to Shiokawa's ACS circuit 5 does provide a suggestion for dynamically controlling squaring circuits 35-39.

Squaring circuits 35-39 simply square the difference value received from subtractors 30-34. The Applicant submits that the notion of "dynamically controlling" the operations of a squaring circuit "based on an error signal generated by the comparator" has no meaning. A squaring circuit is simply not a circuit that is susceptible to such dynamic adaptive control.

The Applicant submits that this provides additional reasons for the allowability of claim 3 (and also claim 16) over the cited prior art.

Claim 7

According to currently amended claim 7, the receiver further comprises one or more adaptive equalizers, each adaptive equalizer configured to receive an ideal data level signal corresponding to one of the data levels and to generate an input signal for one or more of the channel estimators. In rejecting original claim 7, the Examiner cited Shiokawa's adaptive equalizer 1 as an example of the one or more adaptive equalizers of claim 7.

Shiokawa's adaptive equalizer 1 does not receive and process an ideal data level signal corresponding to one of the data levels to generate inputs to channel estimators. Rather, Shiokawa's adaptive equalizer 1 receives and processes the received signal to generate the signal applied to maximum likelihood estimator 2. See input terminal 10 of Fig. 2 and column 2, lines 57-60.

The Applicant submits that this provides additional reasons for the allowability of claim 7 (and therefore claims 8-11 and 20) over Shiokawa.

Claim 10

According to claim 10, each adaptive equalizer is configured to receive one or more future data levels, and the receiver comprises a channel estimator for each different combination of current and future data levels. In rejecting claim 10, the Examiner completely ignored the explicit recitations in claim 10. In fact, Shiokawa provides no such teachings. The Applicant submits that this provides additional reasons for the allowability of claim 10 over Shiokawa.

Claims 12 and 17

According to claim 12, the comparator comprises a subtraction node for each channel estimator and a compare-and-select module. Each subtraction node is configured to generate a difference signal between the received signal and the corresponding estimated signal. The compare-and-select module is configured to receive the difference signals from the subtraction nodes and to select the output data level for the received signal based on a difference signal having a smallest absolute value. As argued previously with regard to claim 1, Shiokawa does not teach these explicit features of claim 12.

In rejecting claim 12, the Examiner stated that “Shiokawa further teaches a subtraction node (between 4 and 5 in Fig. 1).” The Applicant respectfully submits that the Examiner has mischaracterized the teachings of Shiokawa. Frankly, there is absolutely no teaching in Shiokawa about any subtraction nodes between branch metric calculator 4 and add-compare-select circuit 5 in Fig. 1. Rather, the branch metrics B generated by branch metric calculator 4 are provided directly to ACS circuit 5 without any modification and certainly without being applied to any subtraction nodes. See column 4, lines 21-22 (“The outputs of branch metric calculator 4 are fed into the ACS circuit 5.”)

The Examiner also cited ACS circuit 5 as an example of the compare-and-select module of claim 12. According to claim 12, the compare-and-select module selects “the output data level for the received signal based on a difference signal having a smallest absolute value.” The Examiner cited column 4, lines 10-52, of Shiokawa as teaching this feature. Here, too, the Applicant submits that the Examiner has mischaracterized the teachings of Shiokawa. Shiokawa’s ACS circuit 5 performs branch metric calculations to generate logic signals U_1 and U_2 . Significantly, ACS circuit 5 does not “select the output data level for the received signal based on a difference signal having a smallest absolute value.”

The Applicant submits that this provides additional reasons for the allowability of claim 12 (and also claim 17) over Shiokawa.

New Claim 18

According to new claim 18, the model of the transmission channel includes at least one of a 0th order term and a 1st order term. Even if the Examiner’s characterization of the teachings in Shiokawa are correct (which the Applicant does not admit), the fact is that Shiokawa does not teach a model having either 0th or 1st order terms. The Applicant submits that this provides additional reasons for the allowability of claim 18 (and therefore claim 19) over Shiokawa.

New Claim 19

According to new claim 19, each channel estimator comprises a processing path for each order term in the model of the transmission channel. Since claim 18 implies that the model comprises a minimum of two terms (i.e., a 2nd order term and at least one of a 0th and a 1st order term), each channel estimator of claim 19 has at least two processing paths, one for each order term in the model. At best,

Shiokawa teaches channel estimators having a single processing path corresponding to a single (i.e., 2nd order) term. The Applicant submits that this provides additional reasons for the allowability of claim 19 over Shiokawa.

New Claim 20

According to new claim 20, each channel estimator receives a different input signal from the one or more adaptive equalizers. At best, Shiokawa teaches an adaptive equalizer that provides an identical input signal to each different channel estimator. The Applicant submits that this provides additional reasons for the allowability of claim 20 over Shiokawa.

New Claims 21 and 22

New claims 21 and 22 cover the receivers of Figs. 2 and 3, respectively. For many of the reasons given above, the Applicant submits that new claims 21 and 22 are allowable over Shiokawa.

In view of the foregoing, the Applicant submits that the rejections of claims under Sections 102(b) and 103(a) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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